Photo

Name:	Arvind Rajawat
Designation	Professor, Department of ECE, MANIT Bhopal
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Subjects Taught	
U.G	Embedded Systems
	Computer Organization
	Microprocessor
	Integrated Circuits
P.G	Embedded Systems
	VLSI Testing
	VLSI Design
	Computer Networks

Teaching Experience

Organization	Start Date	End Date	Designation	Nature of Work
MANIT Bhopal	January 2012	Till date	Professor	Teaching, UG, PG, PhD supervision, Administrative work, Project execution
	October 2006	Dec 2011	Associate Professor	
	October 2003	October 2006	Assistant Professor	
	October 1998	October 2003	Lecturer Senior scale	
	October 1991	October 1998	Lecturer	

Ph.D Supervised/Ongoing

Name of the Student	Topic	Year of Award	Co-Supervisor (if any)
Sadhna Mishra	Exploring NISC Architecture for Specific Applications	2012	Dr. R. P. Singh
Rajendra Patel	Rapid Design Space Exploration of Instruction Cache Size for Embedded Software	2015	
Mahendra Vucha	On-Chip Dynamic Task Distribution Model for Reconfigurable High Speed Computing System	2016	
Rachna Singh	High Level Area Estimation Model for FPGA based Design	2018	
Abhishek Narain Tripathi	High Level Power Estimation Methodology for FPGA and ASIC based Designs	2020	
Ashish Valuskar	Performance Evaluation Of Network On Chip Architectures	2022	Dr. Madhu Shandilya
Amol Boke	Efficient Design and Implementation of Cryptographic Algorithms Using PUF Key Generators To Secure IoT Devices	2024	Dr. Sangeeta Nakhate
Bharat Singh Chaudhary	CIM based FPGA Architecture	Ongoing	

Sponsored Research Projects (Completed/Ongoing)

Title	Sponsoring Agency	Duration	Amount	Co-PI (if any)
SMDP-C2SD	MEITY, GoI	2015-2021	Rs. 4634363/- (total outlay Rs. 6423820/-)	Dr. Ajay Somkuwar

Publication:

Authors	Title	Journal	Vol. No. Page No.	Year	SCI/Scopus
Amol K. Boke, Sangeeta Nakhate, Arvind Rajawat	*FPGA implementation of PUF based key generator for secure communication in IoT*	Integration	Volume 89 pp 241-247 doi.org/10.1016/j.vlsi.2022.12.006.	2023	SCI
Amol K. Boke, Sangeeta Nakhate, Arvind Rajawat	*An AES Implementation with Improved PDL Based PUF Key Generator for IoT Devices*	*IETE Technical Review*	DOI:10.1080/02564602.2023.2192001	2023	SCI
Boke, A.K., Nakhate, S., Rajawat, A.	Efficient Key Generation Techniques for Securing IoT Communication Protocols	IETE Technical Review	38(3), pp. 282-293	2021	SCI
Abhishek N. Tripathi, Arvind Rajawat	An Accurate and Quick ANN based System-Level Dynamic Power Estimation Model using LLVM IR Profiling for FPGA Designs	IEEE Embedded Systems Letters	vol. 12, no. 2, pp. 58-61 doi 10.1109/LES.2019.2935052	2020	SCI
Abhishek N. Tripathi, Arvind Rajawat	Fast and Accurate System-Level Power Estimation Model for FPGA-Based Designs	Journal of Circuits, Systems and Computers	28(13), doi.org/10.1142/S0218126619502189	2019	SCI
Vaibhav Sharma, Arvind Rajawat	Review of Approaches for Radiation Hardened Combinational Logic in CMOS Silicon Technology	IETE Technical Review	Vol 35 Issue 6 Pages 562-573	2018	SCI
Abhishek N. Tripathi, Arvind Rajawat	Fast and efficient power estimation model for	Microprocessors and Microsystems	Vol. 59, pp 37-45	2018	SCI

	FPGA based designs				
Rachna Singh, Arvind Rajawat	Analytical Model for High-Level Area Estimation of FPGA Design	Embedded and Real-Time Communication Systems	Vol 7, Issue 2, pp 35-44	2016	Scopus
Mahendra Vucha, Arvind Rajawat	Dynamic Task Distribution Model for On-Chip Reconfigurable High Speed Computing System	Reconfigurable Computing	Volume 2015, Article ID 783237 (Open Access Journal, Hindawi Publishing Corporation).	2015	Scopus
Mahendra Vucha, Arvind Rajawat	A Novel Methodology For Task DistributionIn Heterogeneous Reconfigurable Computing System	Embedded Systems and Applications	Vol.5, No.1, pp. 19-39	2015	Google Scholar
Nishant Kumar, Ekta Aggrawal and Arvind Rajawat	Dynamically scalable dual-core pipelined processor	International Journal of Electronics	Volume 102, Issue 10, pp. 1754-1764	2015	SCI
Rajendra Patel, Arvind Rajawat	Recent Trends in Embedded System Software Performance Estimation	Journal of Design Automation for Embedded System	Volume No. 17, Issue 1, pp. 193-213	2013	SCIE
Rajendra Patel, Arvind Rajawat	Dominant Block Guided Optimal Cache Size Estimation to Maximize IPC of Embedded Software	International Journal of Embedded Systems and Applications	Vol. 3, No. 3, pp. 35-44	2013	Google Scholar

Citations

	h-index	i-10 index	Total Citations
Google Scholar	8	5	211

 Administrative positions held: Chairman Council of Wardens, Proctor, Head of the department, Professor

in-charge legal, etc.