Dr. Vibhuti Chauhan

Department of Electronics and Communication Engineering
Maulana Azad National Institute of Technology Bhopal
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EDUCATION

Doctor of Philosophy | *Electronics and Communication Engineering* | July 2019 – February 2024 | *PDPM Indian Institute of Information Technology Design and Manufacturing Jabalpur, M.P.*

- **Thesis Title**: Design Principles of Spacer-based Tri-gate Negative Capacitance FinFET (NC-FinFET) for Low Power Electronics: Simulation and Modelling, CGPA: **9.4/10**

Master of Technology | *Electronics and Communication Engineering* | July 2017 - June 2019 | *PDPM Indian Institute of Information Technology Design and Manufacturing Jabalpur, M.P.*

- **Thesis Title**: Sub-1V Bulk-Driven Ultra-Low power CMOS Operational Transconductance Amplifier, CGPA: **9.4/10**

Bachelor of Technology | *Electronics and Telecommunication Engineering* | July 2013-June 2017 | *College of Engineering Roorkee, Roorkee.*

- Project: Dynamic Threshold Voltage MOSFET (DTMOS) for Low-power VLSI circuits **(83.04 %)**

EXPERIENCE

Assistant Professor Grade-II | *Electronics and Communication Engineering* | November 2024 – ongoing | *Maulana Azad National Institute of Technology, Bhopal*

Assistant Professor | *Electronics and Communication Engineering* | June 2024 – October 2024 | *Bennett University, Greater Noida*

Post-doctoral | *Electrical Engineering* | September 2023 – May 2024 | *Indian Institute of Technology Bombay, Maharashtra*

- **Project Title**: Design Technology Co-optimization of Gate-All-Around Nanosheet structures

COLLABORATION

- **Academia-** IIT Bombay, Georgia Tech US, NIT Bhopal, IIITDM Jabalpur
- **Industry-** Intel, TCAD Synopsys, Micron

AREAS OF INTEREST

- DTCO design of advanced CMOS technologies (Modeling and Simulation)
- Ferroelectric devices, Negative Capacitance phenomena
- Low-power and High-performance VLSI applications
- Reliability analysis (BTI, HCD, SHE, etc.)

TEACHING EXPERIENCE

- Digital Electronics
- Fundamentals of Electronics and Electrical Engineering
- IT Workshop Lab- TCAD Sentaurus, EDA Cadence
- VHDL Programming

HONORS AND AWARDS

- **Best Paper award** at the 5th International Conference "2023 Devices for Integrated Circuit (DevIC)", held at Kalyani Government Engineering College from 7-8 April, 2023, organized by IEEE KGEC Student Branch Chapter in association with IEEE EDS Kolkata Chapter.
- **Best Young Researcher award** issued by Pandit Deendayal Energy University, Gandhinagar, India in association with Materials Research Society of India (MRSI), Gujarat Chapter, Nov. 2021.
- **Governor's Gold Medal** – 2019 for achieving 1st position in the University in Electronics and Telecommunication Department (B.Tech).
- Fellowship by Ministry of Human Resources Development (MHRD), Government of India for M.Tech and PhD studies.
- Fellowship by College of Engineering Roorkee for achieving various scholar positions during B.Tech.

PUBLICATIONS

- **Patent**

  D. P. Samajdar and **V. Chauhan**, "A Tri-Gate Negative Capacitance FinFET device with Buried Interfacial Oxide layer and its Fabrication Method," ***Indian Patent 441737***, July 31, 2023.

- **Journals**

1. **V. Chauhan** and D. P. Samajdar, "Recent Advances in Negative Capacitance FinFETs for Low Power Applications: A Review", ***IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control***, vol. 68, no. 10, 2021.

2. **V. Chauhan** *et al.,* "A Novel Negative Capacitance FinFET with Ferroelectric Spacer: Proposal and Investigation", ***IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control***, vol. 68, no. 12, 2021.

3. A. Dixit, **V. Chauhan**, *et al.* "Sensitivity Analysis of a Novel Negative Capacitance FinFET for Label-Free Biosensing", ***IEEE Transactions on Electron Devices***, vol. 68, no. 10, 2021.

4. **V. Chauhan** *et al.,* "Exploration and Device Optimization of Dielectric-Ferroelectric Sidewall spacer in Negative Capacitance FinFET", ***IEEE Transactions on Electron Devices,*** vol. 69, no. 9, 2022.

5. **V. Chauhan** *et al.,* "Quasi-analytical Model of Surface Potential and Drain Current for Trigate Negative Capacitance FinFET: A Superposition Approach", ***Semiconductor Science and Technology***, vol. 37, no. 8, 2022.

6. **V. Chauhan** *et al.,* "Demonstration of improved Short Channel Performance Metrics for Ferroelectric Concentric Negative Capacitance FinFET", ***Silicon***, vol.15, 2022.

7. **V. Chauhan** and D. P. Samajdar, "Estimation of Performance Degradation due to Interface Traps in Gate and Spacer Stack of NC-FinFET", ***Semiconductor Science and Technology***, vol. 38, no. 4, 2023.

8. **V. Chauhan** and D. P. Samajdar, "Buried Interfacial Gate Oxide for Tri-gate NC-FinFETs: Approach and Investigation", ***Journal of Physics D: Applied Physics***, vol. 56, *2023.*

9. **V. Chauhan** and D. P. Samajdar, "Impact of Buried Gate Oxide on the Electrical Performance of Negative Capacitance FinFETs: Design Perspectives," **Silicon**, 2024.

- **Conferences and Book chapters**

1. **V. Chauhan** *et al.,* "Demonstration of High-Permittivity Sidewall Spacer in Negative Capacitance FinFET", ***Springer Proceedings in Materials***, vol. 15, 2022.

2. **V. Chauhan** *et al.,* "Performance Evaluation of Buried Gate Oxide based Negative Capacitance FinFETs", ***5th International conference "Devices for Integrated Circuits (DevIC 2023)***, April 7-8, 2023, West Bengal, India.

3. **V. Chauhan** *et al.,* "Performance Investigation of Ferroelectric Spacers for Negative Capacitance FinFETs", ***International Symposium on Materials of the Millennium;***

Emerging Trends and Future Prospects (MMETFP-2021), November 19–21, 2021, Gujarat, India.

4. **V. Chauhan** *et al.,* "Demonstration of Ferroelectric Spacer in Negative Capacitance FinFET", ***11th IEEE CASS Rio Grande DO Sul Workshop***, Sept. 29 – Oct. 01, 2021, Brazil.
5. **V. Chauhan** *et al.,* "Sub-1 V Ultra-Low Power CMOS Operational Transconductance Amplifier" in Micro2019, ***6th International Conference on Microelectronics, Circuits and Systems***, 6-7 July 2019, Kolkata, India.

RECENT WORKSHOPS AND COURSES

- Short-term program on "Modeling and Simulation of Nano-Transistors" conducted by the Department of Electrical Engineering, IIT Kanpur from 17th February – 7th March, 2021.
- 11th IEEE CASS Rio Grande do Sul Workshop, September 29 – October 01, 2021, Brazil.

SKILLS

- **Programming Language:** MATLAB, Verilog
- **Simulation Software:** TCAD Sentaurus, Cadence Virtuoso, Xilinx Vivado, HSPICE
- **Document:** MS-Office, PowerPoint, Visio

PROFESSIONAL SERVICES / ACTIVITIES

Memberships

- IEEE Member, 2024- present.
- IEEE Electron Devices Society Member, 2024- present.
- IEEE Young Professionals Member, 2024-present.
- IEEE Women in Engineering Member, 2024-present.

Peer-Reviewed Services

- IEEE Transactions on Nanotechnology (TNANO), IEEE Transactions on Dielectrics and Electrical Insulation (TDEI), Semiconductor Science and Technology (SST) and Engineering Research Express.
- 2nd IEEE Electron Device Kolkata Conference 2022 (EDKCON 2022).
- IEEE International Conference on Electrical, Electronics, Communication and Computers (ELEXCOM 2023).

Volunteer Services

- Secretary Student Chapter- OPTICA (formerly known as OSA), March 2021 - July 2022.

- Head Women in Engineering Student Chapter- IEEE Nanotechnology Council (IEEE NTC), May 2021 – June 2022.

CO-CURRICULAR ACHIEVEMENTS

- Over the time span of last 16 years, I have represented various institutes and clubs in multiple sports majorly, **Basketball, Badminton, Volleyball**, etc., at **national and state levels**. I will be a great asset for the institute in terms of sports as well.
- I have represented **IIITDM JABALPUR for 6 years** in various sports especially at the **All-India Inter-IIIT sports meet** from 2019-2023 and have individually bagged **6 medals (3-gold medal Basketball, 1 gold medal-Badminton, 1 silver medal- Volleyball, and 1 silver medal- Athletics).**
- I have served as a **captain of the Basketball Girls team for consecutively 6 years** with consistent victories in various tournaments and have been the **Girls contingent leader for IIIT Jabalpur in 2020 and 2023**, with girls bagging almost all the medals.

PERSONAL DETAILS

- Date of Birth: August 17, 1996
- Marital Status: Unmarried
- Correspondance Address: Department of Electronics and Communication Engineering, MANIT BHOPAL, Link Road 3, Near Kali Mata Mandir, Bhopal, Madhya Pradesh-462003
- Permanent Address: Vasu General Store, Opposite SBI ATM, Peeth Bazar, Bahadrabad, Haridwar, Uttarakhand-249402

REFERENCES

- **Dr. D. P. Samajdar**
  Assistant Professor, Ph.D. Supervisor
  Department of Electronics and Communication Engineering
  PDPM Indian Institute of Information Technology Design and Manufacturing Jabalpur, M.P
  Contact: 9477137992
  Email: dip.samajdar@iiitdmj.ac.in
- **Prof. Souvik Mahapatra**
  Professor, PostDoc Mentor
  Department of Electrical Engineering
  Indian Institute of Technology Bombay, Maharashtra
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- **Prof. Puneet Tandon**
  Professor, Advisor
  Department of Mechanical Engineering
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  Contact: 9425324240
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November 22, 2024/ Dr. Vibhuti Chauhan